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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/992,076	11/13/2001	Craig Nemecek	CYPR-CD01210M	4880

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EXAMINER	
PROCTOR, JASON SCOTT	
ART UNIT	**PAPER NUMBER**
2123	

DATE MAILED: 11/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/992,076	NEMECEK, CRAIG	
	Examiner	Art Unit	
	Jason Proctor	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 September 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-20 were rejected in office action dated 1 June 2005. Applicants' response has amended claims 1, 3, 4, 5, 8, 17, and 18. Claims 1-20 have been submitted for reconsideration. Claims 1-20 have been rejected.

Drawings

The Examiner thanks Applicants for submitting drawings to overcome the objections raised in the previous office action, however new corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because replacement drawing sheets must be labeled, in the top margin, "Replacement Sheet". This label is required to prevent the originally submitted drawings from being inadvertently printed in a patent issued from this application.

The previous objections to the drawings have been withdrawn.

Specification

The previous objections to the specification have been withdrawn.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. § 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claims 2 and 16 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which

applicant regards as the invention. Claims 2 and 16 recite the acronym "POD" without first defining the term. The standard language defining its use should accompany the first appearance of the acronym in the claims. The Examiner presumes the intended definition is "external circuit board".

In response, Applicants argue primarily that:

> Applicant submits that a POD, within the context of in circuit emulation (ICE), is a term well-known to one having ordinary skill in the art. Therefore, Claims 2 and 16 overcome the basis for rejection under 35 U.S.C. 112 ¶ 2.

The Examiner respectfully traverses this argument as follows.

The claim recites a "POD", emphasis in original, and therefore appears to recite an undefined acronym. Applicants' response sheds no light on the appropriateness of the previously stated interpretation. The Examiner respectfully submits that both "pod" and "POD" are terms used in the art of in circuit emulation (Please see attached documents cited on form PTO-892). It is unclear from the claim language if Applicants distinguish a "POD" from a "pod" even in the context of in circuit emulation. The previously stated interpretation of this limitation is maintained. Applicants' arguments have been fully considered but have been found unpersuasive.

The previous rejections under 35 U.S.C. § 112, second paragraph, of claims 1, 3, 4, 5, 8, 10, 17, and 18 have been withdrawn.

Claim Rejections - 35 USC § 103

Applicants' arguments regarding the previously applied Profit and Barnett references are moot in light of the new grounds of rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2, 5-11, 13-16, and 18-20 rejected under 35 U.S.C. § 102(b) as being anticipated by US Patent No. 5,371,878 to Coker.

Regarding claims 1 and 15, Coker discloses a system comprising:

A microcontroller installed on a test circuit, wherein the microcontroller includes a first memory and a first CPU [*"Embedded Computer System (ECS)"* (column 1, line 22); *"FIG. 1 shows the target-ECS 12 connected to the system hardware 16 by a bi-directional bus line 14 allowing communication in either direction between the target-ECS and the system hardware."* (column 4, lines 3-8); FIG. 1, references 12, 12a, 12b, 14, and 16];

An ICE (in circuit emulator) including a second memory and a second CPU [FIG. 1, references 32, 28, 28a, 28b, and 30] coupled to a computer system [FIG. 1, references 34 and 36], wherein the ICE emulates the microcontroller [*"The shadow system 28 includes and executes the same software and input signals* [...] *as the target-ECS 12."* (column 4, lines 40-43); *"The shadow system 28 is connected to an ICE 32 via an electrical connection 30."* (column 4, lines 51-52)] and the microcontroller and the ICE run the microcontroller code in lock step [*"By operating on input data with the same*

value, memory location and relative timing as the target-ECS, the shadow system has an execution state at any given time corresponding to a known execution state in the target-ECS and can produce a mirror-image or "shadow" of the target-ECS." (column 3, lines 6-12)];

An interface for coupling the test circuit and the ICE enabling data transmission between the test circuit and the computer system [FIG. 1, references 18, 19, 26, 30, 34, 38, etc.], the computer system configured to compare a content of the first memory against a content of the second memory to verify said lock step (column 3, lines 6-12).

Regarding claims 2 and 16, Coker discloses that the microcontroller is installed on an external circuit board [FIG. 1, reference 10].

Regarding claims 5 and 18, Coker discloses that the first and second memory each include a plurality of register files (column 3, lines 6-12).

Regarding claim 6, Coker discloses that lock step execution is maintained by keeping a first and second program counter in lock step [(column 3, lines 6-12); *"Internal state vectors are defined as the contents of RAM and internal registers, i.e., interrupt and status registers, of both the target-ECS and the shadow system."* (column 8, lines 50-65)].

Regarding claims 7, 8 and 19 Coker discloses that the system supports debugging features, implying to a person of ordinary skill in the art the recited steps (column 4, lines 51-61).

Regarding claims 9-11 and 14, these claims recite methods of using the system of claim 1. Coker discloses the system of claim 1 as shown above, and discloses that the system is used for debugging [*"The ICE 32 is a commercially available system allowing the shadow system 28 to be controlled and debugged."* (column 4, lines 51-61); *"The host system 36 is connected to a permanent storage device 36a capable of storing all data necessary to re-create a real time scenario for debug, verification and development purposes."* (column 9, lines 31-42)]. Coker discloses that lock step execution is maintained by keeping a first and second program counter in lock step [(column 3, lines 6-12); (column 8, lines 50-65)]. Coker discloses saving execution history and a trace buffer (column 3, lines 13-34).

Regarding claims 13 and 20, Coker discloses that the microcontroller is a production microcontroller [*"an ECS normally executes software in which the user interface is implemented as a system interface, e.g., a user interface of a computer controlled microwave oven."* (column 1, lines 29-39)].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. § 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claim 3 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Coker as applied to claim 1 above, and further in view of US Patent No. 6,173,419 to Barnett.

4. Claim 12 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Coker as applied to claim 9 above, and further in view of US Patent No. 6,173,419 to Barnett.

5. Claim 17 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Coker as applied to claim 15 above, and further in view of US Patent No. 6,173,419 to Barnett.

Regarding claims 3, 12 and 17 Coker does not expressly disclose whether the shadow system is implemented using an FPGA.

Barnett teaches an emulation system wherein an FPGA is programmed to emulate a microcontroller (column 5, lines 37-55). Barnett teaches that such a system is advantageous by allowing it to be reconfigured (column 5, lines 31-36).

It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to combine the FPGA emulator taught by Barnett with the system of Coker in order to benefit from well-known advantages of hardware emulation, such as speed, as well as

the advantages of being reconfigurable, as explicitly taught by Barnett. The combination could be achieved by implementing the shadow system of Coker with an FPGA.

6. Claim 4 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Coker as applied to claim 1 above, and further in view of "State of the Art" by Stan Augarten, published 1983 (Augarten)

Regarding claim 4, Coker discloses a first and second memory [FIG. 1, references 12a, 12b, 28a, and 28b]. Coker does not expressly disclose whether these memories are static random access memory.

Augarten discloses that SRAM has been known in the art since 1970. Augarten expressly teaches the advantages of SRAM [*"The charges in static RAMs do not leak away, freeing such chips from the need for periodic refreshing"* ... *"this chip was able to retain, in the space of a single core, many times the amount of information"* (third paragraph)]

It would have been obvious to a person of ordinary skill in the art at the time of Applicants' invention to use the well-known technology of SRAM when implementing the system of Coker in order to produce a system having a memory that does not need periodic refreshing and stores many times the amount of information held by traditional ferro-magnetic core memory.

Conclusion

Art considered pertinent by the examiner but not applied has been cited on form PTO-892. New grounds of rejection have been entered in this action, therefore this action is made NON-FINAL.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (571) 272-3713. The examiner can normally be reached on 8:30 am-4:30 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached at (571) 272-3749. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jason Proctor
Examiner
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